Remarks/Arguments

Applicants thank the Examiner for a thorough and timely examination and for withdrawing the rejections under 35 U.S.C. 112, second paragraph, 35 U.S.C. 101 and 35 U.S.C. 102(b).

Additionally, Applicants thank the Examiner for the courtesy extended to the Applicant's representative during the telephonic interview on September 16, 2009. This Amendment is submitted in view of the interview, taking into account the agreements reached and suggestions made by the Examiner.

I. Status of Claims

Claims 1, 4-16 and 33-34 are currently pending in the application. This amendment amends claim 1, cancels claims 2 and 3, and addresses each point of objection and rejection raised by the Examiner.

The amended claim language finds support in the specification as originally filed. Specifically, claim 1 is now amended to include the features previously recited in dependent claims 2 and 3. No new matter has been added. Accordingly, there are no new issues raised herein that should require any further search and/or consideration. As such, Applicants request the Examiner to favorably reconsider the rejections to claims 1, 4-16 and 33-34.

II. Substance of Interview

The Applicants' agent initiated an interview with the Examiner to discuss the outstanding rejections in the interest of advancing prosecution of the present

application. During the telephonic interview on September 16, 2009, the Applicants' agent proposed amendments to claim 1 for overcoming the 35 U.S.C. 112, 2nd paragraph rejections. While specific amendments were agreed upon during the interview, Applicants have further amended claim 1 herein to advance prosecution of the present application.

No specific agreements were reached with respect to the cited prior art. However, the Examiner indicated that clarification of the claim features that Applicant submits in the above amendments would likely overcome the teachings of the cited art, but that an updated search and further review of the cited art is in order and may prove otherwise.

III. Rejections of the Claims under 35 U.S.C. §112, 2nd Paragraph

Claims 1-16, 33 and 34 are rejected under 35 U.S.C. 112, second paragraph as allegedly failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Particularly, the Examiner states that the phrase "as if the code symbols constitute a perfect 2m * J matrix" is indefinite since recitation of "as if" suggests a hypothetical that never occurs and hence cannot have a real tangible connection to the method. Claim 1 is presently amended to more clearly and distinctly claim the subject matter. In particular, the phrase discussed above is removed from claim 1 and the features of claim 2 are amended into claim 1 to clarify the step of generating an interim address. As such, Applicants respectfully request the Examiner to reconsider and withdraw the rejections of claims 1-16 and 33-34 under 35 U.S.C. 112, second paragraph.

IV. Rejections of the Claims under 35 U.S.C. §103(a)

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over TIA/EIA/IS-2000.2-A-1 in view of Tiedmann et al. (U.S. Patent 6,351,460). Applicants respectfully request reconsideration and withdrawal of these rejections.

As amended herein to include the features previously presented in dependent claim 2, independent claim 1 now recites a step of generating an interim address by bit reversal order (BRO) operation on an index of a code symbol by excluding the last column when the number of the code symbols of the last column is less than a half of 2^m code symbols, and generating the interim address by including the last column when the number of the code symbols of the last column is more than or equal to a half of 2^m code symbols. Additionally, claim 1 is further amended to recite the features previously presented in claim 3, for which no prior art rejection was applied by the Examiner. As such, claim 1 now recites the step of calculating an address compensation factor for compensating the interim address based on the real number of R code symbols written in the last column J by increasing the address compensation factor by one each time a code symbol appears in the last column when the last column has less than a half of 2^m code symbols, and decreasing the address compensation factor by one each time a code symbol is excluded from the last column when the last column has more than or equal to a half of 2^m code symbols. In view of the above amendments, Applicants submit that there is no reasonable combination of the teachings in TIA/EIA/IS-2000.2-A-1 with the teachings of Tiedemann that arrives at or suggests each of the claimed features.

Specifically, Figure 2.1.3.1.4.2.3-1 on page 2-111 of TIA/EIA/IS-2000.2-A-1 and the described steps 1-9 fail to teach the claimed steps of generating an interim address and calculating an address compensation factor for compensating the interim address, especially by considering the number of code symbols in the last column as claimed. TIA/EIA/IS-2000.2-A-1 makes no consideration whatsoever of any remaining bits that do not completely fill the last column of an input matrix. As such, there is no teaching or suggestion in TIA/EIA/IS-2000.2-A-1 of generating an interim address by excluding the last column when the number of the code symbols of the last column is less than a half of 2^m code symbols, and generating the interim address by including the last column when the number of the code symbols of the last column is more than or equal to a half of 2^m code symbols. Further, in view of the above, TIA/EIA/IS-2000.2-A-1 necessarily fails to disclose any step of compensating the interim address based on the real number of R code symbols written in the last column J by increasing the address compensation factor by one each time a code symbol appears in the last column when the last column has less than a half of 2^m code symbols, and decreasing the address compensation factor by one each time a code symbol is excluded from the last column when the last column has more than or equal to a half of 2^m code symbols. As such, there is no reasonable combination of TIA/EIA/IS-2000.2-A-1 and Tiedemann that is capable of teaching or suggesting each of the above features.

Accordingly, Applicants request the Examiner to reconsider and withdraw the rejection of claim 1 under 35 U.S.C. 103(a). Dependent claims 4-16 and 33-34 are

patentable on their own merit, yet are distinguished from the cited art at least by virtue of their dependency from claim 1.

V. Double Patenting Rejection

Claim 1 is rejected on the ground of nonstatutory double patenting over claim 5 of U.S. Patent No. 6,668,350. In view of the amendments to claim 1 presented above, Applicants submit that the present application is clearly distinguished from claim 5 of U.S. Patent No. 6,668,350 and does not attempt to improperly extend the "right to exclude" granted by the patent.

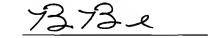
Specifically, Applicants submit that Kim clearly does not disclose or suggest at least the step of calculating an address compensation factor for compensating the interim address to account for the R code symbols written in the last column J by increasing the address compensation factor by one each time a code symbol appears in the last column when the last column has less than a half of 2^m code symbols, and decreasing the address compensation factor by one each time a code symbol is excluded from the last column when the last column has more than or equal to a half of 2^m code symbols.. Kim, however, is directed to an interleaving method in which there are no remaining R bits, as claimed. Thus, any interleaving in Kim is performed with a complete uniform matrix. Since there are no remaining R bits in a last column in Kim, Kim cannot disclose the step of generating a compensation factor based on the remaining R bits. The Examiner states that Kim explicitly recites "calculating a third variable r corresponding to a remainder obtained by dividing a reading sequence K by the second variable J." Such disclosure, however, merely defines the modulo operation which results in the remainder of division of one number by another. The

variable 'r' which is the result of (K mod J) cited in Kim is not related in any way to the remainder R as defined in the preamble of newly amended claim 1. In systems where the number of bit symbols does not enable a uniform matrix in interleaving, it is necessary to compensate for the remaining bits. The present application recites a method of compensating for these remaining bits, thus resulting in the step of address compensation that is neither apparent nor obvious in view of Kim. Since Kim fails to describe or suggest at least these recited features, there is no basis for a double patenting rejection. Applicants respectfully request the Examiner to withdraw the nonstatutory double patenting rejection of claim 1 in view of Kim.

CONCLUSION

In view of the above, it is believed that the above-identified application is in condition for allowance, and notice to that effect is respectfully requested. Should the Examiner have any questions, the Examiner is encouraged to contact the undersigned at the telephone number indicated below. Additionally, Applicants request a one month extension of time under 37 CFR 1.136(a), and submit herewith the applicable fees under 37 C.F.R. §1.17.

Respectfully submitted,



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